CLAIMS:

1. A high speed bit stream data conversion circuit comprising:

a data conversion circuit that receives at least one first bit stream at a first bit rate and a corresponding first bit stream data clock and that produces at least one second bit stream at a second bit rate, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ, wherein the data conversion circuit includes a plurality of drivers used to drive signals based upon the at least one first bit stream and/or the first bit stream data clock; and

a clock circuit that produces a Reference Clock Signal based upon the first bit stream data clock that is used to latch the at least one first bit stream, wherein the clock circuit comprises:

a phase locked loop (PLL) having a phase detector that receives the first bit stream data clock and a loop output, a charge pump, a loop filter, a Voltage Controlled Oscillator (VCO), and a divider that produces the loop output;

wherein the VCO is tuned at an operating frequency corresponding to at least one tuning setting; and

wherein at least some of the plurality of drivers is tuned based upon the at least one tuning setting.

2. The high speed bit stream data conversion circuit of Claim 1, wherein the VCO includes a plurality of switchable tuning capacitors, and wherein the at least one tuning setting comprises switch settings of the plurality of switchable tuning capacitors.

3. The high speed bit stream data conversion circuit of Claim 2, wherein the switchable tuning capacitors comprise coarse tuning capacitors and fine tuning capacitors.

4. The high speed bit stream data conversion circuit of Claim 1, wherein the VCO includes a varactor, and wherein the at least one tuning setting comprises a varactor setting.

5. The high speed bit stream data conversion circuit of Claim 2, wherein the switchable tuning capacitors of the VCO correspond to switchable tuning capacitors of the plurality of drivers, and wherein the VCO and the plurality of drivers are tuned by using consistent switch settings.

6. The high speed bit stream data conversion circuit of Claim 4, wherein the varactor of the VCO corresponds to varactors of the plurality of drivers, and wherein the VCO and the plurality of drivers are tuned by using consistent varactor settings.

7. The high speed bit stream data conversion circuit of Claim 1, wherein the plurality of drivers also serve as buffers.

8. The high speed bit stream data conversion circuit of Claim 1, wherein the VCO further comprises a filter circuit that further comprises a resistor and a capacitor, and wherein the resistor acts to reduce the voltage applied to the VCO.

9. The high speed bit stream data conversion circuit of Claim 1, wherein the data conversion circuit multiplexes the at least one first bit stream into the at least one second bit stream.

10. The high speed bit stream data conversion circuit of Claim 1, wherein the data conversion circuit demultiplexes the at least one first bit stream into the at least one second bit stream.

11. A clock circuit that produces a Reference Clock Signal used to latch data between at least one first bit stream at a corresponding first bit stream data clock and at least one second bit stream, wherein the number and bit rate of the at least one first bit stream and the at least one second bit stream differ, wherein a plurality of drivers drive signals based upon the at least one first bit stream and/or the first bit stream data clock, wherein the clock circuit comprises:

a phase locked loop (PLL) having a phase detector that receives the first bit stream data clock and a loop output, a charge pump, a loop filter, and a

Voltage Controlled Oscillator (VCO), and a divider that produces the loop output, and wherein the VCO is tuned at an operating frequency corresponding to at least one tuning setting; and

wherein at least some of the plurality of drivers is tuned based upon the at least one tuning setting.

12. The clock circuit of Claim 11, wherein the VCO includes a plurality of switchable tuning capacitors, and wherein the at least one tuning setting comprises switch settings of the plurality of switchable tuning capacitors.

13. The clock circuit of Claim 12, wherein the capacitors comprise coarse tuning capacitors and fine tuning capacitors.

14. The clock circuit of Claim 11, wherein the VCO includes a varactor, and wherein the at least one tuning setting comprises a varactor setting.

15. The clock circuit of Claim 12, wherein the switchable tuning capacitors of the VCO correspond to switchable tuning capacitors of the plurality of drivers, and wherein the VCO and the plurality of drivers are tuned by using consistent switch settings.

16. The clock circuit of claim 14, wherein the varactor of the VCO corresponds to varactors of the plurality of drivers, and wherein the VCO and the plurality of drivers are tuned by using consistent varactor settings.

17. The clock circuit of Claim 11, wherein the plurality of drivers also serve as buffers.

18. The clock circuit of Claim 11, wherein the VCO further comprises a filter circuit that further comprises a resistor and a capacitor, and wherein the resistor acts to reduce the voltage applied to the VCO.

19. The clock circuit of Claim 11, wherein the data conversion circuit multiplexes the at least one first bit stream into the at least one second bit stream.

20. The clock circuit of Claim 11, wherein the data conversion circuit demultiplexes the at least one first bit stream into the at least one second bit stream.

21. A method of tuning a plurality of drivers to operate at an operating frequency, comprising the steps of:

tuning a Voltage Controlled Oscillator (VCO) within a Phase Locked Loop (PLL) of a clock circuit to the operating frequency such that such tuning produces at least one tuning setting;

transferring the at least one setting that cause the VCO to operate at the operating frequency to scaled amplifiers within the plurality of drivers that operate on at least one first bit stream and/or at least one second bit stream data at the operating frequency.

22. The method of Claim 21, wherein the VCO includes a plurality of switchable tuning capacitors, and wherein the at least one tuning setting comprises switch settings of the plurality of switchable tuning capacitors.

23. The method of Claim 22, wherein the plurality of switchable tuning capacitors further comprise coarse tuning capacitors and fine tuning capacitors.

24. The method of Claim 22, wherein the VCO includes a varactor, and wherein the at least one tuning setting comprises a varactor setting.

25. The method of Claim 22, wherein the switchable tuning capacitors of the VCO correspond to switchable tuning capacitors of the plurality of drivers, and wherein the VCO and the plurality of drivers are tuned by using consistent switch settings.

26. The method of Claim 22, wherein the varactor of the VCO corresponds to a varactors of the plurality of amplifiers, and wherein the VCO and the plurality of drivers are tuned by using consistent varactor settings.

27. The method of Claim 22, wherein the plurality of drivers also serve as buffers.